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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/732,979

12/11/2003

Axel Brintzinger

2002 P 09238 US

8578

48154

7590

03/24/2006

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EXAMINER

NGUYEN, DILINH P

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/732,979

Applicant(s)

BRINTZINGER, AXEL

Examiner

DiLinh Nguyen

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 8-11, 15-21, 28 and 31-33 is/are pending in the application.
- 4a) Of the above claim(s) 11 and 15-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 8-10, 28 and 31-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election of Embodiment 4 in the reply filed on 12/30/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election of Embodiment 4 (claims 1-5, 8-11, 15-21, 28 and 31-33) is acknowledged. However, claims 11 and 15-21 are directed to a non-elected invention (Embodiment 3). Therefore, claims 11 and 15-21 are withdrawn from consideration as being directed to a non-elected invention.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5, 8-10, 28 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama (U.S. Pat. 6107685) in view Joshi et al. (U.S. Pat. 6731003).

Nishiyama discloses an electronic component comprising:

a wafer 20;

a plurality of bond pads 24 disposed on the wafer;

a plurality of functional 3-D structures (a plurality of bumps are arranged in the middle portion of the wafer 20) disposed on the wafer 20, each functional 3-D structure including a compliant base element; and

a plurality of selected 3-D structures (a plurality of bumps are arranged in the edge region of the wafer) disposed on the wafer to provide a mechanical reinforcement, wherein at least some of the selected 3-D structures have a greater mechanical load-bearing capacity than some of the functional 3-D structures (figs. 2A-2B).

Nishiyama does not disclose a plurality of reroute traces; each reroute trace being electrically connected to one of the bond pad and extending onto a surface of one of the functional 3D structure.

However, Joshi et al. disclose an electronic component comprising a functional 3-D structure and a plurality of reroute traces 24 and 26, each reroute trace being electrically connected to one of the bond pad 32 extending onto a surface of one of the functional 3-D structure (fig. 4, column 3, lines 45-52). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Nishiyama by having a plurality of reroute traces, each reroute trace being electrically connected to one of the bond pad and extending onto a surface of one of the functional 3D structure because as taught by Joshi et al., such the plurality of reroute traces would provide higher resistance and increase likelihood for the semiconductor package (column 6, lines 4-8).

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- Regarding claim 2, Joshi et al. disclose that wherein each reroute trace comprises a nickel layer 24 that is covered by a gold layer 26 (fig. 4, column 3, lines 62-63 and column 4, lines 1-2).
- Regarding claims 3 and 31, Nishiyama et al. disclose that the selected 3-D structures have a greater height than the functional 3-D structures (fig. 2B); therefore, the selected 3-D structures would have a lower degree of compressibility than the functional 3-D structures.
- Regarding claim 4, Nishiyama et al. disclose that the selected 3-D structures (a plurality of bumps are arranged in the edge region of the wafer) have a greater height than the functional 3-D structures (fig. 2B).
- Regarding claim 5, Nishiyama et al. disclose that each of the selected 3-D structures (a plurality of bumps are arranged in the edge region of the wafer) includes a compliant base element that has a significantly greater volume than the compliant base element of the functional 3-D structures (figs. 2A-2B).
- Regarding claims 8 and 32, Nishiyama et al. disclose that the selected 3-D structures (a plurality of bumps are arranged in the edge region of the wafer) are arranged in a regularly distributed manner in an edge region of the wafer 20 (fig. 2A).
- Regarding claims 9 and 33, Nishiyama et al. disclose that the selected 3-D structures are arranged in a regularly distributed manner over the wafer 20 (figs. 2A-2B).

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- Regarding claim 10, Nishiyama et al. disclose that the selected 3-D structures are able to be electrically bonded (fig. 2B).
- Regarding claim 28, Nishiyama discloses an electronic component comprising:
a wafer 20;

a plurality of bond pads 24 disposed on the wafer;
a plurality of functional 3-D structures (a plurality of bumps are arranged in the middle portion of the wafer 20) disposed on the wafer 20, each functional 3-D structure including a compliant base element and having a first height; and

a plurality of other 3-D structures (a plurality of bumps are arranged in the edge region of the wafer) disposed on the wafer to provide a mechanical reinforcement, each of the other 3-D structures having a second height that is greater than the first height (figs. 2A-2B).

Nishiyama does not disclose a plurality of reroute traces, each reroute trace being electrically connected to one of the bond pad and extending onto a surface of one of the functional 3D structure.

However, Joshi et al. disclose an electronic component comprising a functional 3-D structure and a plurality of reroute traces 24 and 26, each reroute trace being electrically connected to one of the bond pad 32 extending onto a surface of one of the functional 3-D structure (fig. 4, column 3, lines 45-52). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Nishiyama by having a plurality of reroute traces, each reroute trace being electrically connected to one of the bond pad and extending onto a surface

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of one of the functional 3D structure because as taught by Joshi et al., such the plurality of reroute traces would provide higher resistance and increase likelihood for the semiconductor package (column 6, lines 4-8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN



HOAI PHAM
PRIMARY EXAMINER